AMITY UNIVERSITY
UTTAR PRADESH

Course Title: Semiconductor Device Physics & Modeling
Course Code: ECE651
Credit Units: 6
Level: PG

L	T	P/ S	SW/F W	TOTAL CREDIT UNITS
3	1	4	0	6

Course Objectives: The general goal of this course is to allow the students to understand the fundamentals of semiconductor behavior and the operation of basic semiconductor devices. Additionally, this course lays the foundations for the understanding of a vast array of other more advanced semiconductor devices such as those covered in more advanced courses. The emphasis of this course will be on a survey of advanced Si and compound semiconductor device physics, especially hetero junctions and metal-semiconductor junctions; high frequency transistors including hetero junction bipolar transistors, JFET's, and MESFET's; and optical devices.

Prerequisites: Basic Electronics Engineering& IC Technology

Course contents/Syllabus:

	Weightage (%)
Module I: Semiconductor & Quantum Mechanics Fundamentals	**20%**
Poisson and continuity equations, Recombination (direct, Auger, trap-assisted), Equilibrium carrier concentrations (electron statistics, density of states, effective mass, bandgap narrowing), Review of PN and MS diodes (Energy Band Diagram). Basic Quantum Mechanics, Crystal symmetry and band structure, 2D/1D density of states, Tunneling.	
Module II: Modeling and Simulation of Carrier Transport	**15%**
Carrier Scattering (impurity, phonon, carrier-carrier, remote/interface), Boltzmann Transport Equation, Monte Carlo, Drift-diffusion phenomenon	
Module III: MOS Capacitors	**15%**
Modes of operation (accumulation, depletion, strong/weak inversion).Capacitance versus voltage. Gated diode. Nonideal effects (poly depletion, surface charges).High field effects (tunneling, breakdown).	
Module IV: MOS Devices	**25%**
Long Channel MOSFET Devices --- Review of operation, I-V characteristics. Subthreshold conduction. Threshold voltage.	

Short Channel MOSFET Devices --- Scaling effects (short channel, narrow channel effects, drain induced barrier lowering) Channel velocity limitations (saturation velocity, interface scattering, mobility models).Hot carrier effects (impact ionization, gate/substrate currents, threshold voltage degradation, velocity overshoot, ballistic effects), Quantum mechanical effects.	
Module V: CMOS Device Designing	**25%**
Scaling relationships, Threshold voltage control, On/Off currents, Channel doping profiles (Implanted channel, buried channel, retrograde wells, S/D extension, HALO/LATID structures) **Advanced Device Technology**-- SOI, SiGe, strained Si, Alternative oxide/gate materials; Alternative geometries (raised source/drain, dual gate, vertical, FinFET)	

Student Learning Outcomes:

- Able to Explain quantum mechanics fundamentals and basic mechanism of electron transport in semiconductor devices.
- Able to Illustrate Energy Band Diagrams
- Able to Identify various modes of operation of MOS capacitors, MOSFETs and methods to improve performance of MOSFETs.
- Able to Evaluate expression of threshold voltage, current etc for MOSFET & its dependence on various physical, electrical and empirical parameters. Able to Analyze performance of different advance device technologies like SOI, SiGe, FinFET etc.

Pedagogy for Course Delivery:

The course would be covered under theory and laboratory. In addition to assigning project–based learning, early exposure to hands-on design to enhance the motivation among the students. It incorporates designing of problems, analysis of solutions submitted by the students groups and how learning objectives were achieved. Continuous evaluation of the students would be covered under quiz, viva etc.

List of Laboratory Experiment

1. Uses a channel implant to shift the threshold voltage of MOSFET by 150 mV (approx.). Analyze the effect of threshold lowering on leakages.
2. To draw the I-V characteristics of HBT.
3. To design and study characteristics of GaAs MESFET.
4. 3D Diode Characteristic.
5. To design GaAs-based high-electron mobility transistor.
6. Enhancement-Mode N-Polar GaN MISFETs.
7. AlGaAs/GaAs HBT Gummel Plot Simulation.
8. High Efficiency Silicon Solar Cell.

9. Luminous Efficiency of a III-V LED Device.
10. Transient Simulation of CMOS Latch-up.

Assessment/ Examination Scheme:

Theory L/T (%)	**Lab/Practical (%)**	**Total**
66.67%	33.33%	100%

Theory Assessment (L&T):

Continuous Assessment/Internal Assessment					**End Term Examination**
Components (Drop down)	Mid-Term Exam	Assignment	Viva	Attendance	
Weightage (%)	10%	7%	8%	5%	70%

Lab Assessment (P):

Continuous Assessment/Internal Assessment					**End Term Examination**
Components (Drop down)	Attendance	PR	LR	Viva	
Weightage (%)	5%	10%	10%	5%	70%

A: Attendance, PR- Performance, LR – Lab Record, V – Viva. EE- External Exam,

Text & References:

- R. F. Pierret, “Semiconductor Device Fundamentals”, Pearson Education, 2008, ISBN: 978-81-7758-977-1.
- R. F. Pierret, “Advanced Semiconductor Fundamentals”, Volume 6 of Modular Series on Solid State Devices, Prentice Hall./Pearson Education, 2003, ISBN: 9780130617927.

- S. Sze, “Physics of Semiconductor Devices”, 3rd Edition, John Wiley and Sons, 2008, ISBN: 978-81-265-1702-2.
- D. A. Neamen ``Semiconductor Physics and Devices", 3rd Edition, Tata McGraw Hill, 2009, ISBN: 978-0-07-061712-4.
- P. Yannis, Tsividis, Colin McAndrew, “Operation and Modeling of the MOS Transistor", 3rd Edition, Oxford University Press, 2011, ISBN: 9780195170153
- Sedra & Smith “Microelectronic Circuits”, 6th Edition, 2010, Oxford University Press, ISBN: 9780195323030